Nokia Customer Care 6255/6255i6256/6256i (RM–19) Mobile Terminal

Baseband Description and Troubleshooting

Contents

Page

ntroduction	4
Power Up and Reset	6
Power Up – Power Key	8
Power Up – Charger Connection	8
Power Up – RTC Alarm	9
Power Off	9
Power Consumption and Operation Modes	9
Power-off Mode	9
Sleep Mode	. 10
Active Mode	. 10
Charging Mode	. 10
Power Distribution	11
Clock Distribution	13
RFClk (19.2MHz Analog)	. 13
RFConvClk (19.2MHz Digital)	. 14
CBUSCIk Interface	. 15
DBUS Clk Interface	. 16
SleepCLK (Digital)	. 17
SleepCLK (Analog)	. 18
Flash Programming	18
Connections to Baseband	. 18
Baseband Power Up	. 18
Flash Programming Indication	. 19
Flashing	. 19
Flash Programming Error Codes	. 22
Charging Operation	24
Battery	. 24
Charging Circuitry	. 24
Charger Detection	. 25
Audio	25
Displays and Keymat	25
Main Display	. 26
Secondary Display	. 27
Keymat	. 27
Camera	27
DC Measurements	. 28
AC Measurements	. 28
FM Radio	29
FM Radio Test	. 29
USB Interface	31
Accessories	33
Charging	. 34
Pop-port Headset Detection	36
FBus Detection	36
Accessory Detection Through ACI	37
RUIM (SIM CAR)	39
Main Display Test Points	. 40

Secondary Display Test Points	45
GPS Module	
Troubleshooting	49
Mobile Terminal is Totally Dead	50
Flash Programming Does Not Work	51
Power Does Not Stay on or the Mobile Terminal is Jammed	53
Charger Faults	55
Audio Faults	56
Earpiece	
Microphone	57
IHF	58
Vibra	59
Display Faults	60
Main Display	60
Secondary Display	62
Keypad Faults	63
Power Key	63
UI Modules	64
EL Panel and Driver	65
USB	66
MMC	70
FM Radio	71
Camera	73
Bluetooth	73
SIM	73
GPS	75

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Introduction

The 6255/6255i/6256/6256i baseband module is a tri-mode, Code Division Multiple Access (CDMA), dual-band engine and is based on the DCT4.5 standard. The baseband engine includes two major Application Specific Integrated Circuits (ASICs):

- D2200 Universal Energy Management Enhanced Integrated Circuit (UEME IC), which includes the audio circuits, charge control, and voltage regulators
- D2800 Main phone processor, which includes system logic for CDMA, two Digital Signal Processors (DSPs), the Main Control Unit (MCU), and the memory

The BL-6C Li-ion battery is used as the main power source and has a nominal capacity of 1070 mA/h.



Figure 1: Baseband block diagram

Power Up and Reset

The UEME ASIC controls the power up and resets. The baseband can be powered up in the following ways:

- Pressing the Power button, which means grounding the PWRONX pin of the UEME
- Connecting the charger to the charger input
- Initiating the Real-time Clock (RTC) alarm, when the RTC logic has been programmed to give an alarm

After receiving one of the above signals (see Figure 2), the UEME counts a 20ms delay and then enters reset mode. The watchdog and VCORE start, and if the battery voltage (VBAT) is greater than Vcoff+, a 200ms delay is started to allow references to settle. After this delay elapses, the VFLASH1 regulator is enabled. Then, 500us later, VR3, VANA, and VIO are enabled. Finally, the Power Up Reset (PURX) line is held low for 20ms. This reset (PURX) is fed to the baseband D2800 processor ASIC, which in turn generates resets for the MCU and the DSP. During this reset phase, the UEME forces the Voltage Controlled Temperature Controlled Oscillator (VCTCXO) regulator on regardless of the status of the sleep control input signal to the UEME.

The FLSRSTx from the UEME is used to reset the flash during power up and to put the flash in power down during sleep mode. All baseband regulators are switched on when the UEME is powered on.

The UEME internal watchdogs are running during the UEME reset state, with the longest watchdog time selected. If the watchdog expires, the UEME returns to the power off state. The UEME watchdogs are internally acknowledged at the rising edge of the PURX signal to always give the same watchdog response time to the MCU.

The following timing diagram represents the UEME start-up sequence from reset to power-on mode.



Figure 2: Power-on sequence and timing



Figure 3: Measured power-on sequence and timing

Power Up – Power Key

When the power key is pressed, the UEME enters the power-up sequence. Pressing the power key grounds the PWRONX pin on the UEME. The UEME PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEME. When the power key is pressed, an interrupt is generated to the D2800 processor that starts the MCU. The MCU then reads the UEME interrupt register through the UEME control bus (CBUS) and notices that it is a PWRONX interrupt. If the PWRONX signal stays low for a certain time, the MCU accepts this as a valid power-on state and continues with the SW initialization of the baseband. If the power key does not indicate a valid power-on situation, the MCU powers off the baseband.

Power Up – Charger Connection

In order to be able to detect and start charging in cases where the main battery is fully discharged (empty), charging is controlled by start-up charging circuitry.

The VBAT voltage level is monitored by the Charge Control Block (CHACON) inside the UEME. When the VBAT level is detected to be below the master reset threshold (V_{MSTR}), charging starts. Connecting a charger forces the Charging Voltage (VCHAR) input to rise above the charger detection threshold (VCH_{DET+}). This causes the UEME to generate

100mA of constant output current from the connected charger's output voltage. The battery's voltage rises at it charges, and when the VBAT voltage level is detected to be higher than master reset threshold limit (V_{MSTR+}), the start-up charge is terminated.

When VBAT is greater than V_{MSTR+} , the Master Output Reset (MSTRX) signal, which is internal to the UEME, is set to a Logic 1. This causes the UEME RESET block to enter into its reset sequence.

If the VBAT is detected to fall below V_{MSTR-} during start-up charging, charging is cancelled. Charging is restarted when a new rising edge on the VCHAR input is detected (VCHAR rising above VCH_{DET+}).

Condition	Result
VBAT < V _{MSTR-} (start-up charging)	Charging starts (VCHAR level begins to rise)
VBAT < V _{MSTR-} (during charging)	Charging is cancelled. A new rising edge of VCHAR (VCHAR $>$ VCH _{DET+}) is required to restart charging
VCHAR > VCH _{DET+}	Battery charges (VCHAR is rising)
VBAT > V _{MSTR+}	Charging ends. MSTRX is set high and the UEME resets.

Table 1: Power-up Sequence through Charger Detection

Power Up – RTC Alarm

If the mobile terminal is in power-off mode when the RTC alarm activates, a wake-up procedure occurs. After the baseband is powered on, an interrupt is given to the MCU. When the RTC alarm occurs during active mode, an interrupt is generated to the MCU.

Power Off

The baseband switches to power-off mode if any of following occurs:

- Power key is pressed
- Battery voltage is too low (VBATT < 3.2V)
- Watchdog timer register expires

The UEME controls the power-down procedure.

Power Consumption and Operation Modes

Power-off Mode

During power-off mode, the power (VBAT) is supplied to the D2800 processor, UEME, MMC, vibra, LED, PA, and PA drivers. During power-off mode, the UEME leakage current consumption is approximately 40uA + 15uA from ZOCOS.

Sleep Mode

When the SLEEPX signal is detected low by the UEME, the mobile terminal enters sleep mode. In sleep mode, both processors (MCU and DSP) are in stand-by mode. The mobile terminal enters sleep mode only when both processors make this request. The following processes occur during sleep mode:

- VIO and VFLASH1 regulators are put into low quiescent current mode
- VCORE enters LDO mode
- VANA and VFLASH2 regulators are disabled
- All RF regulators are disabled
- VCTCXO (19.2MHz clock) is shut down
- 32kHz sleep clock oscillator is used as the baseband reference clock

The average current consumption of the mobile terminal in this mode can vary depending on the software state (e.g., slot cycle 0,1, or 2, and if the mobile terminal is working on IS95 or IS2000 for CDMA). However, on average the current consumption is about 1.3mA in sleep mode and 100mA in active mode.

Sleep mode is exited either by the expiration of a sleep clock counter in the UEME or by some external interrupt (e.g., charger connection, key press, headset connection). Any of these conditions cause a high SLEEPX signal, which is detected by the UEME, and causes the mobile terminal to enter active mode where all functions are activated.

Active Mode

During active mode, the mobile terminal is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. There are several sub-states in the active mode depending on the mobile terminal present state of the mobile terminal, such as burst reception, burst transmission, if the DSP is working, etc.

In active mode, software controls the UEME radio frequency (RF) regulators (VR1A and VR1B), which can be enabled or disabled. These regulators work via the UEME charge pump. VSIM can be enabled or disabled, and its output voltage can be programmed to be 1.8V or 3.0V. VR2 and VR4–VR7 can be enabled, disabled, or forced into low quiescent current mode. VR3 is always enabled in active mode, disabled during sleep mode, and cannot be controlled by the software in the same way as the other regulators. VR3 only turns off if both processors (DSP and MCU) request to be in sleep mode.

Charging Mode

Charging mode can be performed in parallel with any other operating mode. A BSI resistor inside the battery indicates the battery type and size and corresponds to a specific battery capacity.

The battery voltage, temperature, size, and charging current are measured by the UEME and controlled by the Energy Management (EM) charging algorithm.

The charging control circuitry (CHACON) inside the UEME controls the charging current delivered from the charger to the battery. The battery voltage rise is limited by turning the UEME switch off when the battery voltage has reached 4.2V. The charging current is monitored by measuring the voltage drop across a 220mOhm resistor.

Power Distribution

In normal operation, the baseband is powered from the mobile terminal's battery. The battery consists of one Lithium-Ion cell capacity of 1070 mAh and some safety and protection circuits to prevent harm to the battery.

The UEME ASIC controls the power distribution to the entire mobile terminal through the BB and RF regulators. The battery feeds power directly to the following parts of the system:

- UEME
- PA
- Vibra
- Display lights
- Keyboard lights

The heart of the power distribution to the mobile terminal is the UEME. The UEME includes all the voltage regulators and feeds the power to the system. The UEME handles hardware power-up functions so the regulators are not powered and the power-up reset (PURX) is not released if the battery voltage is less than 2.8V.

The baseband is powered from five different UEME regulators (see Table 2):

Regulator	Maximum Current (mA)	Vout (V)	Notes
VCORE DC/DC	300	1.35	The power-up default value is 1.35V. The output voltage is selectable: 1.0V/1.3V/1.5V/1.8V. (Note: If using D2800 processor version 1, the default is 1.57V.)
VIO	150	1.8	Enabled always except during power-off mode
VFLASH1	70	2.78	Enabled always except during power-off mode
VFLASH2	40	2.78	Enabled only when data cable is connected
VANA	80	2.78	Enabled only when the system is awake (off during sleep and power-off modes)
VSIM	25	3.0	Enabled during power-up mode and scanning for a SIM card

Table 2: Baseband Regulators

Table 3 includes the UEME RF regulators.

Regulator	Maximum Current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when cell receiver is on
VR1B	10	4.75	Enabled when the transmitter is on
VR2	100	2.78	Enabled when the transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when the receiver is on
VR5	50	2.78	Enabled when the receiver is on
VR6	50	2.78	Enabled when the transmitter is on
VR7	45	2.78	Enabled when the receiver is on

Table	3:	RF	Regulators
iuoic	•••		negalators

The charge pump that is used by VR1A is constructed around the UEME. The charge pump works with the 1.2MHz clock (CBUS) oscillator and gives a 4.75V regulated output voltage to the RF.

Clock Distribution

RFClk (19.2MHz Analog)

The main clock signal for the baseband is generated from the voltage-controlled temperature-controlled crystal oscillator (VCTCXO). This 19.2MHz clock signal is generated by the radio frequency circuitry and fed to the radio frequency clock (RFCLK) pin of the D2800 processor. The 19.2MHz clock can be stopped during sleep mode by disabling the UEME regulator output (VR3), which in turn powers off the VCTCXO.



Figure 4: Waveform of the 19.2MHz clock (VCTCXO)

RFConvClk (19.2MHz Digital)

The D2800 processor distributes the 19.2MHz clock to the internal processors (the DSP and MCU) where the software multiplies this clock by seven (=134.4MHz) for the DSP and by two (=38.4MHz) for the MCU.



Figure 5: RFCovCLk waveform

CBUSCIk Interface

CBUS utilizes a 1.2MHz clock signal, which is used by the MCU to transfer data between the UEME and the D2800 processor.



Figure 6: CBUS data transfer

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DBUS Clk Interface

DBUS utilizes a 9.6MHz clock signal, which is used by the DSP to transfer data between the UEME and the D2800 processor.



Figure 7: DBUS data transfer

SleepCLK (Digital)

The UEME provides a 32kHz sleep clock for internal use and also to the D2800 processor, where it is used for the sleep-mode timing.



Figure 8: 32 kHz Digital output from UEME

SleepCLK (Analog)

When the system enters sleep mode or power-off mode, the external 32KHz crystal provides a reference to the UEME. The RTC circuit also uses this clock to turn on the mobile terminal during power-off or sleep mode.



Figure 9: 32KHz analog waveform at 32KHz crystal input

Flash Programming

Connections to Baseband

The flash programming equipment is connected to the baseband using test pads for galvanic connection. The test pads are allocated in such a way that they can be accessed when the mobile terminal is already assembled. The flash programming interface includes the VPP, FBUSTX, FBUSRX, MBUS, and BSI signals, which are used by the FLS-8 for flashing. The connection is through the UEME, which means that the logic voltage levels of these signals correspond to 2.78V. Power is supplied to the mobile terminal using the battery contacts.

Baseband Power Up

The baseband power is controlled by the flash prommer in production and in re-programming situations. The baseband powers up by applying supply voltage to the battery terminals. After the baseband is powered up, flash programming indication begins (see the following "Flash Programming Indication" section).

Flash Programming Indication

After connecting the flash prommer to the mobile terminal, the flash prommer sets the MBUS line low to notify the MCU that the flash prommer is connected. This causes the UEME reset state machine to perform a reset to the system by setting the PURX signal low for 20ms.

During flash programming, the MBUS signal transmitted from the UEME to the flash prommer is used as the clock for synchronous communication. This MBUS clock is also supplied by the UEME to the D2800 processor, along with the MBUSRX signal. If the MBUSRX signal is low, the MCU enters flash programming mode. To avoid accidental entry into flash-programming mode, the MCU waits to get input data from the flash prommer. If the timer expires without any data being received, the MCU continues the boot sequence.

When the mobile terminal has entered flash programming mode, the flash prommer writes an 8-bit password to the UEME to indicate that flash programming/ reprogramming is to take place. This 8-bit data is transmitted through the FBUSRX line into a shift register inside the UEME. When the 8 bits have been shifted into the register, the flash prommer generates a falling edge on the BSI line. This loads the shift register content into a comparison register inside the UEME. If the 8 bits in the comparison register matches the default value preset in the UEME, programming starts.

In order to avoid spurious loading of the register, the BSI signal is gated during UEME master reset and during power up when the PURX is active (low). The BSI signal must not change states during normal operation unless the battery is extracted. If the battery is extracted, the BSI signal is pulled high.

Note: A falling edge is required to load the comparison register.

The UEME flash programming mode is valid until the MCU sets a bit in the UEME register that indicates the end of flash programming. Setting this bit also clears the comparison register in the UEME previously loaded at the falling edge of the BSI signal. During the flash programming mode, the UEME watchdogs are disabled. Setting the bit indicating the end of flash programming enables and resets the UEME watchdog timer to its default value. Clearing the flash programming bit also causes the UEME to generate a reset to the D2800 processor.

Flashing

Flash programming is done through the VPP, FBUSTX, FBUSRX, MBUS, and BSI signals.

When the mobile terminal enters flash programming mode, the prommer indicates that flash programming will take place by writing an 8-bit password to the UEME. The prommer sets the BSI value to "1" and then uses FBUSRX for writing and MBUS for clocking. The BSI is then set back to "0".

The MCU uses the FBUSTX signal to indicates to the prommer that it has been noticed. After this, the MCU reports the ID type to the D2800 processor and is ready to receive the secondary boot code to its internal SRAM.



Figure 10: Flashing starts by BSI being pulled up and password being sent to UEME

This boot code asks the MCU to report the mobile terminal's configuration information to the prommer, including the flash device type. The prommer can then select and send the algorithm code to the MCU SRAM and SRAM/Flash self-tests can be executed.



Figure 11: Flashing, continued

- Ch1= PURX
- Ch2 = MBUS toggled three times for MCU initialization
- Ch3 = FBUS_TX low, MCU indicates that prommer has been noticed
- $Ch4 = FBUS_RX$



Figure 12: Flashing, continued 2

Flash Programming Error Codes

The following characteristics apply to the information in Table 4.

- Error codes can be seen from the test results or from Phoenix's flash-tool.
- Underlined information means that the connection under consideration is being used for the first time.

Error	Description	Not Working Properly
C101	"The Phone does not set FbusTx line high after the startup."	Vflash1 VBatt BSI and FbusRX from prommer to UEME. FbusTx from UPP->UEME->Prommer(SAO)
C102	"The Phone does not set FbusTx line low after the line has been high. The Prommer generates this error also when the Phone is not con- nected to the Prommer."	PURX(also to Safari) VR3 Rfclock(VCTCXO->Safari->UPP) Mbus from Prommer->UEME- >UPP(MbusRx)(SA0) FbusTx from UPP->UEME->Prommer(SA1) BSI and FbusRX from prommer to UEME.

Table	4: F	Flash	Programm	ina	Frror	Codes
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Error	Description	Not Working Properly
C103	" Boot serial line fail."	Mbus from Prommer->UEME- >UPP(MbusRx) <u>(SA1)</u> FbusRx from Prommer-> <u>UEME->UPP</u> FbusTx from UPP->UEME->Prommer
C104	"MCU ID message sending failed in the Phone."	FbusTx from UPP->UEME->Prommer
C105	"The Phone has not received Secondary boot codes length bytes correctly."	Mbus from Prommer->UEME->UPP(MbusRx) FbusRx from Prommer->UEME->UPP FbusTx from UPP->UEME->Prommer
C106	"The Phone has not received Secondary code bytes correctly."	Mbus from Prommer->UEME->UPP(MbusRx) FbusRx from Prommer->UEME->UPP FbusTx from UPP->UEME->Prommer
C107	"The Phone MCU can not start Secondary code correctly."	UPP
C586	"The erasing status response from the Phone informs about fail."	Flash
C686	"The programming status response from the Phone informs about fail."	Flash
Cx81	"The Prommer has detected a checksum error in the message, which it has received from the Phone."	FbusTx from UPP->UEME->Prommer
Cx82	"The Prommer has detected a wrong ID byte in the message, which it has received from the Phone."	FbusTx from UPP->UEME->Prommer
A204	"The flash manufacturer and device IDs in the existing algorithm files do not match with the IDs received from the target phone."	Flash UPP VIO/VANA Signals between LIPP-Flash
Cx83	"The Prommer has not received phone acknowledge to the message."	Mbus from Prommer->UEME->UPP(MbusRx) FbusRx from Prommer->UEME->UPP
Cx84	"The phone has generated NAK signal during data block transfer."	
Cx85	"Data block handling timeout"	
Cx87	"Wrong MCU ID."	RFClock UPP(Vcore)
Startup for flashing	Required startup for flashing	Vflash1 VBatt

Table 4: Flash Programming Error Codes (Continued)

Charging Operation

Battery

The mobile terminal uses a Lithium-Ion cell battery (BL-6C) with a capacity of 1070mAh. Reading a resistor inside the battery pack on the BSI line indicates the battery size. An NTC resistor close to the SIM connector measures the mobile terminal's temperature on the BTEMP line. Temperature and capacity information are needed for charge control. These resistors are connected to the BSI pins on the UEM. The mobile terminal has 100K Ω pull-up resistors for these lines so that they can be read by A/D inputs in the mobile terminal.



Figure 13: BL-5C battery pack pin order

Charging Circuitry

The UEME ASIC controls charging depending on the charger being used and the battery size. External components are needed for Electromagnetic Compliance (EMC), reverse polarity, and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The baseband is designed to support DCT3 and higher chargers from an electrical point of view. Both 2- and 3-wire type chargers are supported. However, the 3-wire charger is treated as a 2-wire charger.



Figure 14: Charging circuitry

Charger Detection

Connecting a charger creates voltage on the VCHAR input of the UEME. Charging starts when the UEME detects the VCHAR input voltage level above 2 V (VCH_{det+} threshold). The VCHARDET signal is generated to indicate the presence of the charger for the SW. The EM SW controls the charger identification/acceptance.

The charger recognition is initiated when the EM SW receives a "charger connected" interrupt. The algorithm basically consists of the following 3 steps:

- 1. Check that the charger output (voltage and current) is within safety limits.
- 2. Identify the charger as a 2-wire or 3-wire charger.
- 3. Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.



Figure 15: Charging circuit

Audio

The audio control and processing is provided by the UEME, which contains the audio codec, and by the D2800 processor, which contains the MCU and DSP blocks. These blocks handle and process the audio data signals.

The baseband supports three microphone inputs and two earpiece outputs. The microphone inputs are MIC1, MIC2, and MIC3:

- MIC1 is used for the mobile terminal's internal microphone
- MIC2 is used for headsets (HDB-4)
- MIC3 is used for the Universal Headset

Every microphone input can have either a differential or single-ended AC connection to the UEME circuit. The internal microphone (MIC1) and external microphone (MIC2) for Pop-portTM accessory detection are both differential. However, the Universal Headset interface is single-ended. The microphone signals from different sources are connected to separate inputs at the UEME. Inputs for the microphone signals are differential types. Also, MICB1 is used for MIC1 and MICB2 is used for MIC2 and MIC3 (Universal Headset).

Displays and Keymat

The mobile terminal utilizes the main display and a secondary display, as well as an electroluminescent (EL) panel for the keymat lighting.

Main Display

There are three LEDs for the main display, which utilize the KLIGHT signal. Table 5 shows the characteristics of the main display.

Parameter	Value
Technology	Active matrix (TFD)
Resolution	160 x 128
Number of LEDs	4
Number of colors	64K
Interface	Messi-8 (parallel)
Illumination mode	White (default)

Table 5: Main Display Characteristics





Figure 16: Waveform for the main display interface

Secondary Display

There are three LEDs for the secondary display, which utilize the DLIGHT signal. Table 5 shows the characteristics of the secondary display.

Parameter	Value
Technology	Passive (C-STN)
Resolution	96 x 65
Number of LEDs	3
Number of colors	4096
Interface	LoSSI (serial)
Illumination mode	Black (default)

Table 6: Secondary Display Characteristics

Keymat

An EL panel is used for keymat illumination, which is controlled by the GPIO(57) signal.

Camera

The following block diagram shows the camera and HWA connections to the baseband.



Figure 17: Camera and HWA connections to the baseband

DC Measurements

Signal Name	Measured Value (V)	Min	Typical	Max	Unit	Description
VIO	1.8	1.7	1.8	1.9	V	Control line
VANA (Vflash2)	2.79	2.7	2.78	2.9	V	Analogue supply
VDIG	1.79	1.7	1.8	1.9	V	Digital supply
GND	0		0		V	System GND

Table 7: Power Supply Characteristics

Table 8: DC Characteristics

Signal Name	Measured Value (V)	Min	Typical	Max	Unit	Description
CSX	H = 1.80 L = 2.0m	H = 0.7xVI0 L = 0		H = VI0 L: 0.3xVI0	V	Camera chip select (active low)
DaClk	H = 1.77 L = -18m	H = 0.7xVI0 L = 0		H= VIO L= 0.3xVIO	V	Voltage levels
TxDa	H = 1.75 L = -18m	H = 0.8xVI0 L = 0		H = VI0 L = 0.2xVI0	V	Data to transmit, camera interrupt (active low)
RxDa	H = 1.76 L = -11m	H = 0.7xVI0 L = 0		H = VI0 L = 0.3xVI0	V	Data to receive
ExtClk	H = 1.75 L = -12m	0.5Vp-p	1Vр-р	VIOp-p	V	All modes
VCtrl	N/A	H = 0.7xVI0 L = 0		H = VI0 L = 0.3xVI0	V	Logic 0: shutdown

Note: H stands for high signal level and L for low signal level.

AC Measurements

Signal Name	Measured Value (V)	Min	Typical	Max	Unit	Description
DaCLK	F = 4.799	4.69	4.8	4.81	MHz	Frequency
	D = 49.4	45/55	50/50	55/45	%	Duty cycle
ExtClk	F = 9.6	9.59	9.6	9.69	MHz	External system clock (mode 4)
	D = 49.3	45/55	50/50	45/55	%	

Table	9: AC	Measurement	Characteristics
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Note: DaClk frequency will not exceed ExtClk/2

FM Radio

FM radio circuitry is implemented using highly integrated radio IC, TEA5767HN. FM radio circuitry is controlled through the serial bus (GenIOs) interface from MCU SW.



Figure 18: FM Radio (N356), Audio (N150), antenna, and digital interface connections

Stereo audio output signals are fed to the stereo amplifier. Volume control of the FM audio signal is made by circuitry inside the amplifier. The amplified audio signal is fed to the headset or IHF speaker. The headset is also used as an antenna input for the radio.

FM Radio Test

To hear the FM radio, connect the headset to the Pop-port or UHJ ports because the headset is the FM radio antenna. Also, connect the headset to an UHJ port to control the FM radio using Phoenix. However, if you connect a headset (e.g., HDS-3) to a Pop-port connector, then you cannot control the mobile terminal because you have already occupied the connection port (Pop-port). In this case you have to have jumper wires on the production test points (Fbus Tx/RX, GND).

Input Signals to the FM Radio

After connecting a headset to the UHJ port to control the mobile terminal through Phoenix, you can see the following signals by turning on the FM radio in Phoenix (which is in the RF menu).

Check the following signals to see whether they are changed as represented in Figure 19:

- FMClk = Test Point (FM04) : 32KHz/1.8V
- FMWrEn = Test Point (FM03) : Write enable at 1.8V
- FMCtrlClk = Test Point (FM02) : Control clock at 1.8V
- FMCtrlDa = Test Point (FM01) : Control data at 1.8V



Figure 19: FM Radio signals before Radio on

- Ch1 : FMClk(32.768KHz)
- Ch2 : FMWrEn
- Ch3 : FMctrlClk
- Ch4 : FMctrlDA



Figure 20: FM Radio signals after Radio on

USB Interface

The USB (Universal Serial Bus) allows up to 127 devices to be attached via a tree-like structure of hubs and devices all emanating from one root host. Devices can be attached or detached at any time without concern for rebooting the PC or loading device driver software. Detection of attachment or detachment is done automatically and requires no user input.

The mobile terminal is a full speed peripheral device, and as such, communicates with the host PC at 12Mbps. Full speed USB allows for fast transfer of large data formats (MP3, JPEG, AVI, etc.). When the mobile terminal is used as a modem, a fast interconnect with the PC is required.

The mobile terminal incorporates the portal USB engine. This engine is supported using an ASIC core supplied by TI. This core is called the Wireless Function Controller 2 (W2FC) and is included in the D2800 processor IC. The core completes several USB functions automatically and is controlled by the ARM9 MCU.

Because the D2800 processor's IO cells are restricted to 1.8V, the Nokia USB Transceiver (NUT) is used as a data-level, shifting and conditioning ASIC. NUT provides the interface between the ASIC's 1.8V bus and the 3.3V USB bus. Before the USB signals are passed to the system connector, they pass through an Application Specific Integrated Passive (ASIP) that integrates five passive components and provides >8kV ESD protection for the external data and power supply lines.

Issue 2 05/2005

NOKIA



The USB consists of four signals:

Table 10:	USB Signals
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Signal	Description
Vbus	5V Power supply from host to device
D+	Differential data signal (swings between 0 and +3.3V)
D-	Differential data signal (swings between 0 and +3.3V)
GND	Ties host and device ground together

When the mobile terminal is attached to a USB host, the host provides a 5V supply at the Vbus pin of the system connector. The NUT indicates the presence of the host to the W2FC by altering the state of Vp and Vm as shown in Table 11.

Vcc	Vp	Vm
0V	Logic 1	Logic 1
5V	Same logic as D+	Same logic as D-

Table 11: Vp and Vm States

After the USB host is connected, D+ and D- are pulled to GND by 15kW resistors at the host end. In turn, the Vp and Vm are pulled low. Any state other than Vp=Vm=1 generates a wake request interrupt. When the NMP software receives this interrupt, it enables the 48MHz clock and wakes the MCU from deep sleep.

When the NMP software is ready to communicate with the USB host, it asserts the 1.3kW pull up on the D+ signal by instructing the W2FC to assert its PUENO signal. The NUT detects this and ties the D+ signal to a 3.3V supply through the 1.3kW pull up. The W2FC brings the NUT out of suspend by setting SUSPEND low. The NUT now draws the majority of its current from the USB host 5V supply.

The USB host detects a high state on the D+ line and recognizes that a USB device is attached. 100ms later, the USB host drives a reset for 10ms by driving D+ and D- low. Following the reset, the USB host starts to drive data across the D+ and D- lines, requesting configuration information from the device. The NUT level shifts and conditions this data, presenting it to the W2FC on its RCV, Vp and Vm pins.

Once the W2FC has decoded the received data, it begins transmitting back to the USB host by asserting the NUT's active low OE pin and then driving data on the NUT's VO pin. After some level shifting and conditioning, the NUT drives the D+ and D- lines with this data.

The USB Tx and Rx continue in this fashion controlled by the USB host.

Accessories

The 6255/6255i/6256/6256i supports Pop-port and Universal Headset accessories, differential and single-ended, respectively. Detection of the Pop-port accessories is done through the ACI signal where the Universal Headset is detected on TIKU_GenIO (4).



Figure 22: Pop-port connector pin out

The pin out on the Pop-port connector is as follows:

- Charger
- Charger GND
- ACI
- Vout
- USB Vbus
- USB D+ / Fbus Rx
- USB D- / Fbus Tx
- Data GND
- XMic N
- XMic P
- HSear N
- HSear P
- HSear R N
- HSear R P

You can perform the following in Pop-port accessories:

- Charging
- Accessory detection
- FBUS communication
- USB communication
- Fully differential audio interface for mono- and stereo outputs

Charging

Charging through Pop-port is accomplished in the same manner as through the charger connector. Pin 1 of the Pop-port is physically connected to the charger connector. When the mobile terminal is connected to a desktop charger (e.g., DCV-15), it charges in the same manner as it does with the charger connector.

Figure 23 shows the actual charging sequence. The channels on the diagram are:

- CH1 = Charging current across the .22 Ohm (R200) resistor on UEMEK
- CH2 = Charger voltage measure at V100
- CH3 = Battery voltage measure at R200



Figure 23: Charging sequence

In Channel 4, PURX is released, which this indicates when the mobile terminal operation goes from RESET mode to POWER_ON mode.
Pop-port Headset Detection

Accessory detection on the Pop-port is done digitally. The pins used for this accessory detection are:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)



Figure 24: Waveform showing Pop-port accessory detection

FBus Detection

FBus communication in Pop-port is done through the following lines:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)
- Pin 6 (FBus Rx)
- Pin 7 (FBus Tx)



Figure 25: Waveform showing Pop-port FBus communication

Accessory Detection Through ACI

USB and Audio on (mono or stereo)/FM radio communication in Pop-port is done through the following signals:

USB	Audio/FM
Pin 5 (USB Vbus)	Pin 9 (XMic N)
Pin 6 (USB +)	Pin 10 (SMIC P)
Pin 7 (USB -)	Pin 11 (HSEAR N)
Pin 8 (Data GND)	Pin 12 (HSEAR P)
	Pin 13 (HSEAR R N)
	Pin 14 (HSEAR R P)

Tabla	12.	Accord	Detection	Ciana	I۰
raule	12:	Accessory	Detection	Signa	IS



Figure 26: Waveform showing accessory detection through ACI

RUIM (SIM CAR)

The 6255/6255i/6256i/6256i supports SIM CAR. Use the waveform in Figure 27 to verify that the sim_vcc, sim_i/o, cim_clk, and sim_rst signals are activated in the correct sequence at power up. This picture may be taken when the SIM CAR is installed on the mobile terminal to measure the signals when the mobile terminal is turned on. The figure shows the proper waveforms when the interface is working. See Figure 28 on page 41 for the test point's location.



Figure 27: RUIM signal waveform

Main Display Test Points



Figure 28: Main display test points - top



Figure 29: Main display test points - bottom - 1

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Figure 30: Main display test points - bottom - 2



Figure 31: Main display test points - bottom - 3

Secondary Display Test Points



Figure 32: Secondary display test points - top



Figure 33: Secondary display test points - bottom - 1

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Figure 34: Secondary display test points - bottom - 2

GPS Module

The GPS circuitry utilizes RF signals from satellites stationed in geosynchronous orbit to determine longitude and latitude of the handset. The GPS circuitry is completely separate of the CE circuitry and is located almost exclusively on the secondary side of the PWB underneath the display module.



Figure 35: GPS Block Diagram

Use the following steps for basic GPS BB troubleshooting:

- 1. Always perform a visual inspection on the GPS circuitry to see if the problem is physical (dislodged parts, corrosion, poor solder joints, etc.) before performing a diagnostic test.
- 2. Put the GE and CE in the proper mode
- 3. Check to make sure that necessary inputs from the CE are good (power, clock, etc.).
- 4. Ensure that these inputs produce the proper outputs.

Because of the large level of integration (most functionality is contained in the two ASIC chips), the amount of diagnostics one is able to do is limited.

Troubleshooting

The following hints allow you to find the cause of the problem when the circuitry seems to be faulty. Troubleshooting instructions are divided into the following sections:

- Mobile terminal is totally dead
- Flash programming does not work
- Power does not stay on or the mobile terminal is jammed
- Charger faults
- Audio faults
- Display faults
- Keypad faults
- USB
- MMC
- FM Radio
- Camera
- Bluetooth
- SIM
- GPS

First, carry out a through visual check of the module. Ensure in particular that:

- There are no mechanical damages
- Soldered joints are okay
- ASIC orientations are okay

Mobile Terminal is Totally Dead



Flash Programming Does Not Work





Power Does Not Stay on or the Mobile Terminal is Jammed





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Charger Faults



Audio Faults



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Microphone



Audio faults, page 3 **Check IHF audio** amplifier Is IHF working? NO-NO-Replace N2100. (N2100). Is it OK? YES ¥ Set the phone to Local Mode. Use Phoenix to open Troubleshooting > Phone Control > Phone State tab > Check R117, select Local Mode > click Execute. R2118, R2119. If Then use Audio test > HP NO -OK, change the microphone in/ Ext speaker out > UEMEK. Loop ON. Measure and check IHF YES test points IHFA and IHFB. Are they OK? YES ¥ Change IHF speaker. Audio faults, page 4

IHF

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Vibra



Display Faults





Secondary Display



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Keypad Faults



UI Modules



EL Panel and Driver



USB

Before proceeding with the USB faults troubleshooting portion of this guide, attach a DKU-2 cable between the mobile terminal and the PC. The PC must recognize that a USB device has been attached and load driver(s) for that device. The mobile terminal appears in the **Device Manager** dialog box.



Figure 36: Device Manager dialog box

If the mobile terminal appears, the USB device detection protocol is functioning and indicates this is not a hardware fault. No further troubleshooting is possible.

If no device is detected, proceed as follows:







MMC

The hardware of the MMC interface from the UEME (D2200) to the MMC connector (X3200) cannot be tested without an MMC card. Solder wires on respective points to be able to measure the following.



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FM Radio FM Radio faults Check solder on Power on the phone Is the FM radio N6100, X101, and and turn FM radio on NO-NO--replace N6100 if not working? by Phoenix working. YES ¥ **Measure VFlash2** NO YES (VCCD/VCCA/ VCCVCO) at C6103/ NO-► **Check VFlash2 line** C6116/C6117/L6101. Is it 2.8V? YES Does the FM radio produce a "Bong" Measure FM1=1.8V, sound when Change TikuEDGE FM2=11 Khz, NOchanging channels D2800 FM3=1.8V, and (frequencies)? FM4=32 Khz. Is it OK? YES Check L6102, L6103, V YES NO Check soldering C6104, C6109, V under C6100, R6101, C6115, C2008, R6103, C6102. If not C2009, C2010, Measure FMANT at NOworking, then C2011. If OK, check L6103. Is it 1.0V? change FM radio Tomahawk chip (N6100). connector (X2000) on pin 11, 12, 13, 14 YES V (From Radio Faults 2) FM END Radio NO faults 2


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Camera



Bluetooth

See the RF Troubleshooting chapter for Bluetooth troubleshooting information. When the flash D450 or UEME have been replaced the ESN has to be reprogrammed. This automatically includes reprogramming the BT address.

SIM

The hardware of the SIM interface from the UEME (D2200) to the SIM connector (X2700) can be tested without a SIM card. When the power is switched on, the mobile terminal checks for a 1.8V SIM card and then a 3V SIM card. The mobile terminal attempts this four times, whereafter it displays "Insert SIM card".

The error "SIM card rejected" means that the ATR message received from the SIM card is corrupted (e.g., data signal levels are wrong). The first data is always ATR, and it is sent from the card to the mobile terminal.



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GPS



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